REMARKS

Claims 8-12, 14-17, and 19-20 are now pending.

In the Final Rejection dated November 17, 2003, the Examiner rejected claims 8, 14, 15, and 16 under 35 U.S.C. § 103(a) as being unpatentable over Hiroyuki et al JP 2000-188369 (Hiroyuki) in view of Takiar et al U.S. Patent No. 5,422,435 (Takiar), and claims 9 and 10 under 35 U.S.C. § 103(a) as being unpatentable over Hiroyuki in view of Takiar and further in view of Lau, Flip Chip Technologies, (Lau). The Applicants traverse these rejections as follows.

A key teaching of the present invention is the formation of a miniaturized semiconductor device employing a stacked multi-chip package (MCP), using flip-chip bonding technology in the lower chip of the stack to effectively improve productivity and broaden chip size options. In the prior art, it has been difficult to thin the overall semiconductor device of this type because of the multiplicity of chips in the stack.

One prior art method for thinning the stacked MCP is thinning all chips uniformly, such as is disclosed in the secondary reference to Takiar. The Takiar patent discloses that each semiconductor chip has an even thickness, without discussing the effect of bonding pressure.

Hiroyuki (corresponding to Juso, U.S. Patent No. 6,181,002) discloses another prior art idea in which, among the plurality of semiconductor chips in the stack, the semiconductor chip having the largest plan surface area has the greatest thickness. For this reason, Hiroyuki discloses that the flip-chip-bonded chip is thinner than the wire-bonded chip simply because the plan surface area of the flip-chip-bonded chip is less than that of the wire-bonded chip. Significantly, Hiroyuki is concerned with stresses due to thermal effects of mold resin sealing, specifically warpage and cracks, but does not discuss the effects of bonding pressure.

In the flip-chip bonding step of the present invention, electrically connecting all of the protruding electrodes of a semiconductor chip simultaneously with corresponding electrodes of a wiring substrate while applying pressure to the back surface of the semiconductor chip requires a high-pressure application to assure a high yield of connections between the electrodes, because all connections are provided simultaneously. Moreover, a sufficient thickness of the chip to which the pressure is applied is necessary to carry out the bonding. However, if all chips are thickened uniformly in the stacked MCP, or if the decision about which chips should have

greater or lesser thickness is based on plan surface area, it is difficult to appropriately reduce the total thickness of the semiconductor device because either a) all chips would require the thickness necessary for the chip undergoing the back pressure, resulting in a greater overall thickness of the stacked MCP, or b) the overall thickness of the stacked MCP is determined by the chip having greatest plan surface area, whether it is the pressure-applied chip, respectively. In the invention as claimed in claim 8, the relative thicknesses of the first and second semiconductor chips is consistently defined in accordance with which chip receives the pressure to its back surface (i.e., the first semiconductor chip). By this method, the first semiconductor chip is sufficiently thick to sustain the high pressure, whereas the thickness of the second semiconductor chip, bonded via adhesive, is reduced to thereby reduce the overall thickness of the stacked MCP, without sacrificing yield.

Moreover, as previously argued, the combination of Hiroyuki and Takiar does not teach the pressure-electrical connection of the protruding electrodes with the corresponding electrodes of the wiring substrate. Although the Examiner asserts that the Applicants attack the references individually in an inappropriate manner, in fact, the Applicants attack

each reference individually to show that neither reference teaches that for which the combination is allegedly applied. In particular, neither Hiroyuki nor Takiar teaches to make the necessary electrode connections via pressurization. The Examiner has argued that Takiar's teaching of soft solder bonding of chips is "relevant" to the flip-chip bonding of the present claims. However, the Examiner does not explain how the person of ordinary skill can be led to the claimed bonding by two references, neither of which teaches the claimed pressurized bonding. Even Takiar, allegedly teaching this feature, utilizes wire bonding, as noted by the Examiner on page 3 of the Final Rejection.

Concerning independent claims 17 and 20, the generation of voids on the main surface of the second semiconductor chip can be suppressed in accordance with the claimed preparation of a mold having a plurality of resin injection entrances created on a first side surface thereof and a ventilation hole created on a second side surface, facing the first side surface, thereof. By this step, the flow of resin is directed as shown in Figure 29A, redirecting the resin with ease to a space above the main surface of the second semiconductor chip so that air in the cavity is expelled from the ventilation

hole. Hiroyuki does not teach this feature of the claimed invention.

In view of the foregoing amendments and remarks, the Applicants request reconsideration and reexamination of the rejection and allowance of the claims.

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Date: February 17, 2004